Our Docket No.: 042390.P6725

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Altug Koker et al.	Examiner: Jasmine Song
Application No.: 09/372,296	Art Group: 2187
Filed: August 11, 1999	
For: REDUCING MEMORY ACCESS LATENCIES FROM A BUS USING PRE-FETCHING AND CACHING	

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231-9999

Dear Sir:

Applicants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicants also submit herewith our check number 12850 in the amount of $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f). Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666.

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-21 of the present application are pending and remain rejected. The applicants hereby appeal the rejection of claims 1-21.

IV. STATUS OF AMENDMENTS

The Applicant filed an amendment on December 23, 2002, in response to a Final Office Action issued by the Examiner on October 23, 2002. In response to the December 23, 2002 remarks, the Examiner issued an Advisory Action on January 16, 2003. The applicant filed a Notice of Appeal from the Advisory Action on January 23, 2003.

The response filed December 23, 2002 was referred to as an amendment. However, because the response did not actually contain any request to amend any portion of the application, the response ~~was filed December 23, 2002~~ was considered a request for reconsideration and was ~~interpretted~~ interpreted as such in the advisory action ~~dated~~ mailed January 16, 2003.

V. SUMMARY OF INVENTION

The present invention discloses a technique to reduce memory access latencies from a bus using prefetching and caching. A bus access circuit 125 includes a peripheral bus controller 210, a pre-fetcher 215, a cache controller 230, a data coherence controller 250, a scheduler 260, a data mover 270, and a cache queue 280. The pre-fetcher 215 includes a request packet generator (RPG) 220, a watermark monitor 225, and a request queue (RQ) 240. These functional blocks are closely coupled together but perform isolated functions in a pipeline manner to provide high throughout and reduce bus access latencies.[1]

The peripheral bus controller (PBC) 210 receives control and request signals from the peripheral bus and interfaces to the pre-fetcher 215 and the cache controller (CC) 230. The PBC 210 decodes the access request and determines if the access request is valid. If the access request is valid, the PBC 210 forwards the access request to the RPG 220 and to the CC 230. The CC 230 determines if there is a hit or a miss. The RPG 220 returns a control signal to the PBC 210 for moving data from the cache queue 280 to the peripheral bus. Upon receipt of the control signal from the RPG 220, the PBC 210 sends a command to the CC 230 to start the data transfer from the cache queue 280 to the peripheral bus.[2]

The pre-fetcher 215 generates packet requests to a memory controller which provides access to the memory.[3]

The cache controller (CC) 230 receives control information from the PBC 210 and interacts with the watermark monitor 225, the data mover 270, and the cache queue 280. The CC 230 manages the data allocation for the cache queue 280 by monitoring the amount of data in the

[1] See Specification, page 7, lines 16-22.
[2] See Specification, page 7, lines 23-25, page 8, lines 1-8
[3] See Specification, page 8, lines 9-10.

cache queue 280. This information is forwarded to the data mover 270 for controlling data movement from the memory to the cache queue 280.[4]

The request queue (RQ) 240 stores the access requests as generated by the RPG 220 to optimize the transactions between the memory units and the bus units. The RQ 240 allows the memory units and the bus units to operate independently.[5]

The data coherence controller (DCC) 250 receives a control signal, (e.g., a clear data signal), from the RPG 220 and forwards to the control signal to the data mover 270, which in turn forwards to the CC 230.[6]

The scheduler 260 keeps track of the read packets that are sent to the memory controller. The scheduler 260 receives the request packets from the RQ 240 and sends the request packets to the data mover 270 when the memory units return a data item.[7]

The data mover (DM) 270 transfers the data from the memory to the bus.[8]

The cache queue (CQ) 280 stores data items from the memory as transferred by the DM 270. The amount of data in the CQ 280 is monitored by the CC 230. The data items stored in the CQ 280 are read out to the peripheral bus when the CC 230 determines that there is a hit upon receiving a read request from the bus as generated by the PBC 210, or when the missed data are transferred from the memory to the CQ 280.[9]

Data items are moved into and transferred out of the CQ280 according to a first in first out manner such that the sequence of data move is the same as the sequence of data delivery. [10]

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[4] See Specification, page 9, lines 5-10.
[5] See Specification, page 5, lines 14-16.
[6] See Specification, page 9, lines 21-23.
[7] See Specification, page 10, lines 1-4.
[8] See Specification, page 10, line 11.
[9] See Specification, page 10, lines 18-23.
[10] See Specification, page 12, lines 1-6, page 13, lines 1-6, lines 18-24, page 4, lines 1-10, lines 19-24, page 15, lines 1-11, Figure 3A, 3B, 4A and 4B.

VI. ISSUES

The issues are:

(i) whether Claims 1, 4-5, 8 and 15 are unpatentable under 35 U.S.C. § 102(e) over U.S. Patent No. 6,216,208 issued to Greiner et al. ("Greiner").

(ii) whether Claims 2-3, 9-12 and 16-19 are unpatentable under 35 U.S.C. § 103(a) over Greiner in view of U.S. Patent No. 6,356,962 issued to Kasper ("Kasper"), and whether Claims 6-7, 13-14, and 20-21 are unpatentable under 35 U.S.C. § 103(a) over Greiner in view of official notice.

VII. GROUPING OF CLAIMS

Applicant contends that the claims of the present invention stand or fall together. In other words, claims 1, 4-5, 8, and 15, and claims 2-3, 9-12 and 16-19, and claims 6-7, 13-14, and 20-21 form a single group.

VIII. ARGUMENTS

A. Claims 1, 4-5, 8, and 15 are not anticipated by the prior art

In the Office Action, the Examiner rejected claims 1, 4-5, 8 and 15 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6216208 issued to Greiner et al. ("Greiner"). Applicants respectfully disagree and submit that the Examiner has not made a prima facie showing that Claims 1, 4-5, 8, and 15 are anticipated by the cited reference. The cited reference do not disclose, either explicitly or inherently, or suggest (1) a prefetcher to prefetch data from a memory to a data queue, and (2) a queue controller to deliver the perfetched data from the data queue to a bus independently of the memory.

Greiner discloses a prefetch queue responsive to read request sequences. A processor includes a bus sequencing unit (BSU) and a core. An external bus interconnects the processor with other components such as memories (Greiner, col. 2, lines 10-16). The BSU includes an internal cache memory, an internal queue, and a prefetch queue (Greiner, col. 2, lines 17-19). The internal queue monitors requests and informs the prefetch queue of read requests (Greiner, col. 2, lines 61-63). The prefetch queue includes an address buffer to store addresses associated with previous read requests (Greiner, col. 3, lines 28-31). The objective is to determine if the read requests exhibit a pattern indicating that the core is reading from sequential locations in external memory (Greiner, col. 3, lines 1-4).

Greiner does not disclose, either expressly or inherently, a prefetcher to prefetch data from a memory to a data queue and a queue controller to deliver the perfetched data from the data queue to a bus independently of the memory. As clearly shown in Figure 2 in Greiner, the prefetch queue receives the address information from the internal queue, not from a memory. Furthermore, the element 162 is an address buffer to store addresses associated with the request, not the data (Greiner, col. 3, lines 28-31).

In the advisory action dated January 16, 2003, the Examiner stated that the above limitation is taught as "the cache controller coupled to the cache deliver the prefetched data to the core without resorting to the slower external bus which is the system memory (col.5, lines 54-58)". (Advisory Action, Page 2). This argument is flawed for a number of reasons. First, Greiner taught that the prefetched data are obtained by receiving the address information from the internal queue, not from the memory as claimed ("prefetching a plurality of data from a memory to a data queue"). Second, as disclosed by Greiner, the data are delivered to the core,

not to a bus independently of the memory as claimed ("delivering the pre-fetched data from the data queue to a bus independently of the memory").

In the advisory action, the Examiner further stated that the element 162 in Greiner stores the data associated with the request (Greiner, Col. 3, lines 56-58). Applicants respectfully disagree. The term "data" as used in Greiner is to refer to the information to be written to or read from. The element 162 is an address buffer that stores addresses as explicitly taught by Greiner: "The entry buffers store addresses associated with previous read requests." (Greiner, Col. 3, lines 27-31).

In the Advisory Action, the Examiner stated that the addresses received by the internal queue represent the physical address in the external memory (Greiner, Col. 2, lines 66-67; Col. 3, line 1). However, the question is not whether the address in the internal queue representing the physical address. The question is whether the prefetcher prefetches the data from a memory to a data queue. Applicant contends that Greiner does not disclose, either inherently or expressly, prefetching data from a memory to a data queue in response to a request. First, Greiner merely teaches that the prefetch queue prefetches from the next location in the sequence in the internal queue when a certain pattern arise (Greiner, Col. 3, lines 4-5), not in response to a request. Second, Greiner does not disclose prefetching data from a memory to a data queue. There is no data queue in Greiner.

To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Since the Examiner failed to show that Greiner teaches or discloses any one of the above elements, the rejection under 35 U.S.C. §102 is improper.

B. Claims 2-3, 6-7, 9-14 and 16-21 are unobvious over the prior art

In the Office Action, the Examiner rejected claims 2-3, 9-12 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over Greiner in view of U.S. Patent No. 6356962 issued to Kasper et al. ("Kasper"). The Examiner further rejected claims 6-7, 13-14, and 20-21 under 35 U.S.C.

§103(a) as being unpatentable over Greiner in view of official notice. Applicants respectfully traverse the rejection for the following reasons.

Greiner discloses a prefetch queue responsive to read request sequences. Greiner, as discussed above, does not disclose a prefetcher to prefetch data from a memory to a data queue.

Kasper discloses a network device and method of controlling flow of data arranged in frames in a data-based network. A look-ahead watermark functions as a synchronizing signal in a FIFO memory structure to indicate that sufficient storage exists to receive more bursts (Kasper, col. 3, lines 35-39).

Here, there is no motivation to combine Greiner and Kasper because neither of them addresses the problem of reducing memory access latencies from a bus. There is no teaching or suggestion that a prefetcher to prefetch data from a memory to a data queue is present. Greiner and Kasper, read as a whole, does not suggest the desirability of prefetching data from a memory to a data queue and delivering the prefetched data to a bus independently of the memory.

In addition, there is no motivation to modify Greiner according to official notice. Greiner does not disclose, suggest, or render obvious prefetching data from a memory to a data queue and delivering the prefetched data to a bus independently of the memory. The Examiner argued that the peripheral component interconnect (PCI) bus is well known in the art and therefore it would have been obvious to one of ordinary skill in the art to use the PCI bus in Greiner's bus system. However, the very fact the PCI bus was well known in the art at the time of Greiner but was not taught by Greiner indicates that it was not obvious to modify Greiner.

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 U.S.P.Q. (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the

Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 U.S.P.Q.2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

Therefore, Applicants believe that independent claims 1, 8 and 15 and their respective dependent claims are distinguishable over the cited prior art references.

C. Conclusion

The Federal Circuit stated that to anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Furthermore, The Federal Circuit stated that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 947 F.2d. 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Furthermore, M.P.E.P. § 2142 states that:

> "To establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Neither one of Greiner and Kasper discloses or suggest: (1) pre-fetching a plurality of data from a memory to a data queue in response to a request, and (2) delivering the pre-fetched data from the data queue to a bus independently of the memory.

As a result, none of the cited references discloses, suggests, or renders obvious the present invention as recited in Claims 1-21.

Applicants respectfully request that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated or rendered obvious by the prior art.

Respectfully submitted,

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Dated April 23, 2003

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (TWICE AMENDED) A method comprising:

pre-fetching a plurality of data from a memory to a data queue in response to a request; and

delivering the pre-fetched data from the data queue to a bus independently of the memory.

2. (AMENDED) The method of claim 1 wherein pre-fetching comprises:

determining if an amount of data in the data queue is above a predetermined level; and

placing the request to a memory controller controlling the memory if the amount of data is not above the predetermined level, the request causing the memory controller to transfer the plurality of data to the data queue, the request being buffered in a request queue.

3. (AMENDED) The method of claim 2 wherein the delivering comprises:

transferring the data from the data queue to the bus if the data in the data queue is ready.

4. The method of claim 1 further comprising:

determining if the request is valid; and

processing a cache miss request if the request results in a cache miss.

5. The method of claim 4 wherein the processing of the cache miss request comprises:

providing a purge signal;

marking an entry in a scheduler according to the purge signal;

purging data corresponding to the marked entry; and

placing the request to the memory controller.

6. The method of claim 5 wherein the bus is a peripheral component interconnect (PCI) bus.

7. The method of claim 6 wherein the request is one of a 32-byte and a 64-byte requests.

8. (TWICE AMENDED) An apparatus comprising:

a pre-fetcher to pre-fetch a plurality of data from a memory to a data queue in response to a request; and

a queue controller coupled to the data queue and the pre-fetcher to deliver the pre-fetched data from the data queue to a bus independently of the memory.

9. (AMENDED) The apparatus of claim 8 wherein the pre-fetcher comprises:

a watermark monitor to determine if an amount of data in the data queue is above a predetermined level;

a request packet generator coupled to the watermark monitor to place the request to a memory controller controlling the memory if the amount of data is not above the predetermined level, the request causing the memory controller to transfer the plurality of data to the data queue; and

a request queue coupled to the request packet generator to store the request provided by the request packet generator.

10. (AMENDED) The apparatus of claim 9 wherein the queue controller transfers the data from the data queue to the bus if the data in the data queue is ready.

11. (AMENDED) The apparatus of claim 9 further comprising:

a peripheral bus controller coupled to the bus and the pre-fetcher to determine if the request is valid;

a data coherence controller coupled to the pre-fetcher to provide a purge signal when the request corresponds to a cache miss; and

a scheduler coupled to the request queue and the data coherence controller to store entries corresponding to the request, the entries being marked according to the purge signal from the data coherence controller.

12. (AMENDED) The apparatus of claim 11 further comprising:

a data mover coupled to the data queue and the scheduler to transfer data from the memory to the data queue, the data mover purging data corresponding to a marked entry from the scheduler.

13. The apparatus of claim 12 wherein the bus is a peripheral component interconnect (PCI) bus.

14. The apparatus of claim 13 wherein the request is one of a 32-byte and a 64-byte requests.

15. (TWICE AMENDED) A system comprising:

a memory;

a bus; and

a bus access circuit coupled to the memory and the bus to reduce latency in accessing the memory from the bus, the bus access circuit including:

a pre-fetcher to pre-fetch a plurality of data from the memory to a data queue in response to a request, and

a queue controller coupled to the data queue and the pre-fetcher to deliver the pre-fetched data from the data queue to the bus independently of the memory.

16. (TWICE AMENDED) The system of claim 15 wherein the pre-fetcher comprises:

a watermark monitor to determine if an amount of data in the data queue is above a predetermined level;

a request packet generator coupled to the watermark monitor to place the request to a memory controller controlling the memory if the amount of data is not above the predetermined level, the request causing the memory controller to transfer the plurality of data to the data queue; and

a request queue coupled to the request packet generator to store the request provided by the request packet generator.

17. (AMENDED) The system of claim 16 wherein the queue controller transfers the data from the data queue to the bus if the data in the data queue is ready.

18. (AMENDED) The system of claim 16 wherein the bus access circuit further comprises:

a peripheral bus controller coupled to the bus and the pre-fetcher to determine if the request is valid;

a data coherence controller coupled to the pre-fetcher to provide a purge signal when the request corresponds to a cache miss; and

a scheduler coupled to the request queue and the data coherence controller to store entries corresponding to the request, the entries being marked according to the purge signal from the data coherence controller.

19. (AMENDED) The system of claim 18 wherein the bus access circuit further comprising:

a data mover coupled to the data queue and the scheduler to transfer data from the memory to the data queue, the data mover purging data corresponding to a marked entry from the scheduler.

20. The system of claim 19 wherein the bus is a peripheral component interconnect (PCI) bus.

21. The system of claim 20 wherein the request is one of a 32-byte and a 64-byte requests.